IN THE SPECIFICATION

Please replace paragraph 0020 with as follows:

The detector circuit 74 indicates when an object is close to the electrode. When a conductive object is close to electrode 14 (Figure 1) modeled by electrode circuit 72, the detector circuit 74 senses a voltage drop at second node 73 with respect to the reference voltage at first node 71. A differential operational amplifier 86 uses the voltage at first node 71 as its inverting input and the voltage at second node 73 as its noninverting input. In an alternative, the second node 73 can be the inverting input and the first node 71 [as] the noninverting input. The output 80 is coupled to a diode D_1 for conversion to a DC output 82 indicating an object is in close proximity. A sample hold capacitor C_5 connected to diode D_1 reduces noise in DC output 82. The closer the object to the electrode 14, the larger electric field attenuation as indicated by a drop in the DC output 82. The DC output 82 is coupled to a controller 84 with addresses 92. One suitable programmable integrated circuit for the controller 84 is the Microchip PIC16F77 made by Microchip Technology, Inc. in San Jose, CA, which performs logic to analyze DC output 82 as described below.

Please replace paragraph 0023 with as follows:

In another embodiment shown in Figure 5, the address scheme can be used on a keypad such as keypad 75 on an electric field proximity keyboard 67 by nesting the row and column addresses to form a larger array of electrodes. For example, the electric field keyboard 67 is defined by an array of keypads with three rows ($m_1 = 3$) and four columns ($n_1 = 4$) such as the keypads 75, 76, 77, and 78, where each of the keypads such as keypad 75 is further defined by an array with three rows [($m_{2=3}$)] ($m_2 = 3$) and four columns [($n_{2=4}$)] ($n_2 = 4$) of electrode pairs. The electric field proximity keyboard 67 includes a total of 12 ($m_1 \times n_1$) keypads and a total of ($m_2 \times n_2$) 12 electrode pairs associated with each keypad such as keypad 75. Thus, the address scheme has a total of 144 ($m_1 \times n_1$) x ($m_2 \times n_2$) electrode pairs but only 25 ($m_1 \times m_2$) + ($n_1 \times n_2$) I/O addresses.